PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re U.S. Patent No. 6,750,701 B2	)	Serial No. 10/052,779
Inventor(s): Atsushi KAWASUMI	)	Filed: January 23, 2002
Issue Date: June 15, 2004	)	Attorney Docket No. 005405.00004

For: CURRENT MIRROR CIRCUIT AND CURRENT SOURCE CIRCUIT

REQUEST FOR CERTIFICATE OF CORRECTION

U.S. Patent and Trademark Office
Customer Service Window
Randolph Building, Mail Stop: Certificate of Correction Branch
401 Dulany Street
Alexandria, VA 22314

Sir:

Pursuant to 35 U.S.C. § 254 and 37 C.F.R. § 1.322, this is a request for the issuance of a Certificate of Correction in the above-identified patent. Two (2) copies of PTO Form 1050 are appended. The complete Certificate of Correction involves one page.

The mistake identified in the appended Form occurred through no fault of the Applicant, as clearly disclosed by the records of the application, which matured into this patent. Enclosed for your convenience are the relevant portions of an Amendment which was filed December 13, 2002.

Issuance of the Certificate of Correction containing the correction is respectfully requested. Since this change is necessitated through no fault of the Applicant, no fee is believed to be associated with this request. Nonetheless, should the Patent and Trademark Office determine that a fee is required, please charge our Deposit Account No. 19-0733.

Respectfully submitted,

BANNER & WITCOFF, LTD.

Dated: March 16, 2005

By: _____
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UNITED STATES PATENT AND TRADEMARK OFFICE

CERTIFICATE OF CORRECTION

PATENT NO.: 6,750,701 B2

DATED: June 15, 2004

INVENTOR(S): Atsushi KAWASUMI

It is certified that an error appears in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

In the claims: Column 10, Claim 4, Line 26
"PMQS" should be replaced with --PMOS--.

Mailing Address of Sender:

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Washington, DC 20001-4597

FORM PTO 1050 (Rev.2-93)

U.S. PAT. NO 6,750,701

No. of add'l copies
@ 504 per page

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MAR 2 5 2005

☒ PATENT ☐ DESIGN B&W Ref. 005405.00004 Date 12-13-02

☐ HAND CARRY Group/Section _____ Bldg _____ Rm _____

Serial/Patent No. 10/052,779 Atty/Sec WFR/jab

Inventor KAWASUMI Client MIYOSHI

Title _____

The following has been received in the U.S. Patent and Trademark Office on the date stamped hereon:

☐ _____total pp Spec., including : # of Claims _____
(# of independent claims _____): ☐ Abstract

☐ Drawings : ☐ Formal ☐ Informal
# of distinct sheets _____: Figs. _____

☐ Declaration/Power of Attorney : ☐ Executed ☐ Unexecuted

☐ Assignment w/PTO Cover Sheet

☐ IDS w/PTO 1449 ☐ References ☐ w/Fee

☐ Preliminary Amendment

☐ Priority Claim (Foreign or U.S. Provisional. B&W # _____)

Country Appl. # Date

☐ w/Foreign Priority Document(s)

☐ Application : ☐ CIP ☐ Continuation ☐ Divisional
Parent Ser. No. _____ B&W# _____

☐ U.S. Provisional _____pp Spec/Claims; Cover Sheet

☐ Response to Missing Parts/Requirements dtd _____

☐ Response to Notice to File Corrected Appln. Papers dtd _____

☐ Request for Expedited Foreign Filing License

☐ Request for Corrected : ☐ Filing Receipt ☐ Assignment

☐ Response to Restriction/Election Requirement

16

☐ Sequence Listing : ☐ Diskette ☐ Paper

☒ Amendment ☐ Response : OA dtd _____

☐ Petition for Extension of Time until _____

☐ CPA ☒ RCE ☐ w/Ext of Time : OA dtd 9-13-02

☐ Request for Approval of Drawing Changes

☐ Notice of Appeal & Fee

☐ Brief : ☐ Appeal & Fee ☐ Reply

☐ Request for Oral Hearing

☐ Issue Fee ☐ Advance Patent Copies (# ordered _____)
Notice of Allowance dtd _____

☐ Amendment under 37 CFR 1.312

☐ Request for Certificate of Correction

☐ Transmittal ☐ Fee Transmittal w/Auth. to Charge Deposit Acct.

☐ Certificate of Mailing

☐ Check #_____ for $ _____

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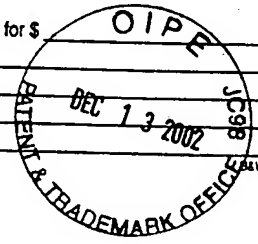

B&W Rev. 5/01

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In Re Application Of:	)	
	)	Group Art Unit: 2816
Atsushi Kawasumi	)	
	)	Examiner: T. Cunningham
Appln. No.: 10/052,779	)	
	)	
Filed: January 23, 2002	)	
	)	
For: Current Mirror Circuit And Current Source Circuit	)	Atty. Dkt. No. 005405.00004
	)	Confirmation No.: 7218

The Honorable Assistant Commissioner for Patents
Washington, D.C. 20231

Sir:

AMENDMENT ACCOMPANYING REQUEST FOR CONTINUED EXAMINATION UNDER 37 C.F.R. § 1.114

Pursuant to 37 C.F.R. § 1.114 and in response to the Final Office Action dated September 13, 2002, Applicant respectfully requests continued examination of this application. A separate Request for Continued Examination and the associated fees are filed concurrently herewith.

Prior to further examination, please amend the above-identified application as follows:

IN THE CLAIMS:

Please cancel claims 12-15 without prejudice or disclaimer.

Please amend claims 2, 9, 17, 19, 21, and 22 into the following form:

2. (Twice Amended) A current mirror circuit comprising:

a current source;

a first MOS transistor having a gate, a drain coupled to the gate and the current source, and a source coupled to a first power source;

at least one subtracter coupled to the drain of the first PMOS transistor and the second PMOS transistor, each subtracter configured to supply a voltage which is higher than the voltage V_{gs} to the gate-source of each compensation PMOS transistor.

17. (Twice Amended) A current mirror circuit comprising:

a current source;

a first group of PMOS transistors connected in series, the first group of PMOS transistors including:

a first PMOS transistor having a gate, a drain coupled to the gate, and a source, wherein the source of the first PMOS transistor is coupled to a first power source, wherein the first PMOS transistor is defined as being electrically closest to the first power source in the first group of PMOS transistors, and

a second PMOS transistor having a gate, a drain coupled to the gate, and a source, wherein the drain of the second PMOS transistor is coupled to the current source, wherein the second PMOS transistor is defined as being electrically closest to the current source in the first group of PMOS transistors;

a second group of PMOS transistors connected in series, wherein the number of PMOS transistors in the second group of PMOS transistors is equal to the number of PMOS transistors in the first group of PMOS transistors, the second group of PMOS transistors including:

a third PMOS transistor having a gate coupled to the gate of the first PMOS transistor, a drain, and a source, wherein the source of the third PMOS transistor is coupled